FIG.1
BACKGROUND ART 20 گ ADDRESS QUEUE OUTPUT#1 OUTPUT#2 OUTPUT#3 OUTPUT#4 INPUT PORTS OUTPUT PORTS #1 #1 #2 #2 CELL-COPY CIRCUIT #3 #3 #4 #4 DEMUX MUX ζ_{30} 410 MULTICAST CELL WITH DESTINATION OUTPUT PORTS #1,#3, AND #4

FIG.2
BACKGROUND ART

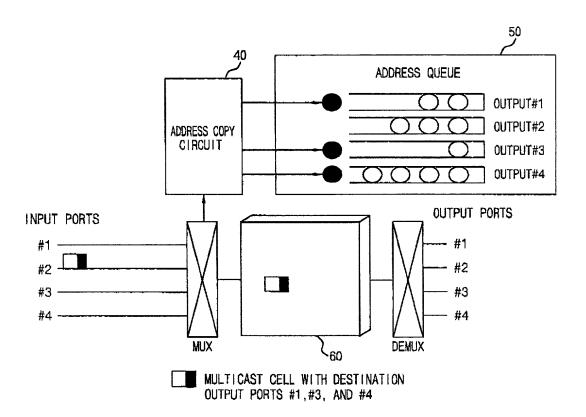
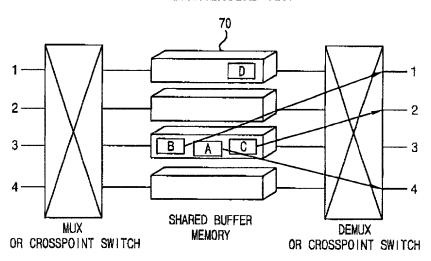


FIG.3
BACKGROUND ART



	ADDRESS QUEUE	
OUTPUT PORT #1		
OUTPUT PORT #2		IDLE STATE PRODUCED BY HOL BLOCKING
OUTPUT PORT #3		BY HUL BLUCKING
OUTPUT PORT #4		
TAIL	HEAD	

FIG.4

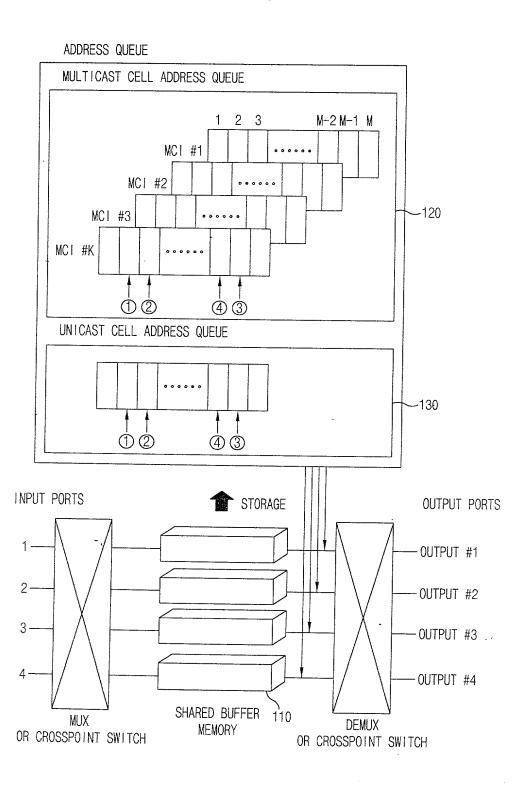


FIG.5

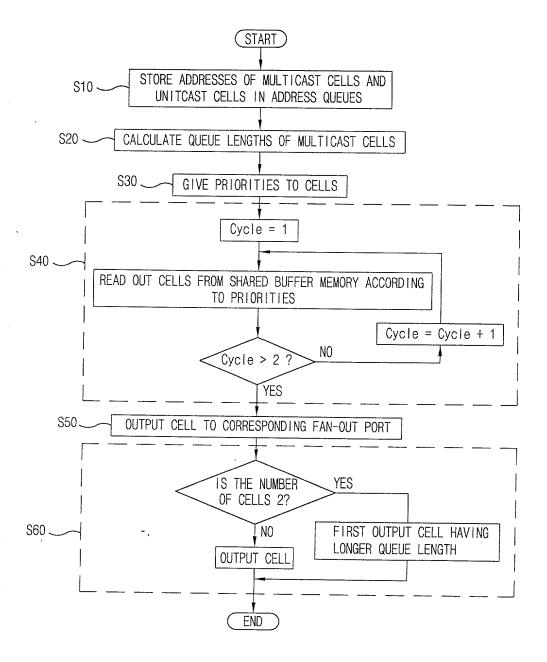


FIG.6

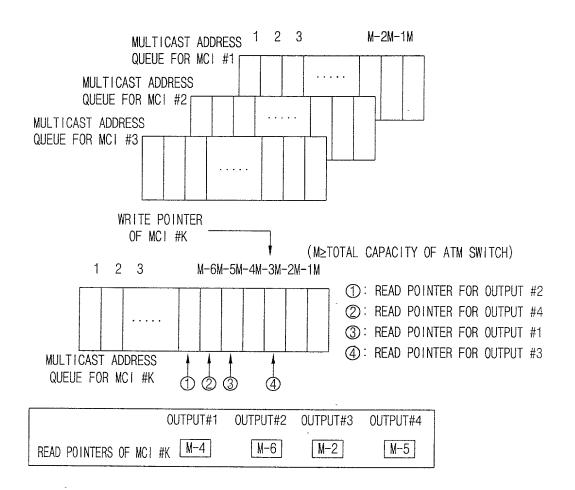


FIG.7A

	OUTPUT #1	OUTPUT #2	OUTPUT #3	OUTPUT #4
MCI #1 ADDRESS QUEUE	89	88	90	84
MCI #2 ADDRESS QUEUE	91	95	80	83
MAXIMUM QUEUE LENGTH	91	95	90	84
PRIORITY	2	1	3	4

FIG.7B

		OUTPUT PORT				
READ PRIORITY		1	2	3	4	
	1st		-	SBM #4(s ₁)		
	2nd	SBM #2(s ₂)				
	3rd		SBM #2(s ₃)			
	4th				SBM #2(s ₄)	

OUTPUT PORT & READ PRIORITY OF UNICAST CELL(s)

FIG.7C

OUTPUT PORT 1 2 3 4 1st SBM #2(m₁) 2nd SBM #3(m₂) 3rd SBM #4(m₃) 4th SBM #4(m₄)

QUEUE LENGTH OF m1 : 95

QUEUE LENGTH OF m2 : 91 QUEUE LENGTH OF m3 : 90

QUEUE LENGTH OF m4 : 84

OUTPUT PORT & READ PRIORITY OF MULTICAST CELL(m)

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